Guía de QUARTUS

En esta práctica de laboratorio se va a implementar un circuito lógico en un dispositivo lógico programable utilizando como CAD (Computer aided design) el Quartus II de Altera (disponible la versión estudiante en www.altera.com) y como programador el kit de educación UP1 o UP2 también de Altera.

Pasos a seguir

1) Comienzo

Crear un directorio para guardar todos los archivos correspondientes a cada proyecto.

To create a new project:

Choose New Project Wizard (File menu). The New Project Wizard appears. The first time you open the New Project Wizard, it may display the Introduction page; you can click Next to proceed to the first page of the wizard.

Type the directory name in the working directory box, or select the directory with Browse (...). For this example, type d:\altera\qdesigns<version number>\fir_filter or browse to select it.

Type a name for the project in the project name box. Type filtref as the name of the top-level design entity of the project in the top-level design entity box.

Click Next. The Add Files page of the New Project Wizard appears. Because is a new project, there are no files to add to this project yet. If design files already existed for this project, you could use Browse (...) to select the files, and then click Add to add them to the project.

To accept the default settings for the remaining wizard prompts and create the project, click Finish. The project is now created. The top-level design entity name appears in the Hierarchy tab of the Project Navigator window

2a) Diseño gráfico: Block diagram (.bdf)

A BDF can contain block symbols and "ordinary" schematic symbols. The Quartus II software provides symbols for a variety of logic functions—including primitives, Library of Parameterized Modules (LPM) functions, and other megafunctions—that you can use in the Block Editor

Choose New (File menu). The Device Design Files tab of the New dialog box appears automatically.

Select Block Diagram/Schematic File.

Click OK. A new Block Editor window opens.

Choose Save As (File menu). The Save As dialog box appears.

Select the folder where you want to save the BDF. The Save As dialog box should automatically display the project directory name, d:\altera\qdesigns<version number>\fir_filter, as the directory for saving the file.

Make sure Add file to current project is turned on.

To save the file and add it to the project, click Save.

Double-click any empty space in the Block Editor window. The Symbol dialog box appears.

In the Libraries list, click the + icon to expand the d:/altera/quartus<version number>/libraries folder. Similarly, expand the primitives folder, and then expand the storage folder.

In the storage folder, select any primitive. A preview of the new symbol appears in the Symbol dialog box.

Click OK. An outline of the the symbol is now attached to the pointer.

Click the pointer at the desired location in the Block Editor window to insert the symbol into the design file.

You can change the **Block Editor display options**, as needed. To change the Block Editor display options, follow these steps:

Choose Options (Tools menu). The General page of the Options dialog box is displayed.

In the Category list, select Block/Symbol Editor. The Block/Symbol Editor page appears.

In the Block/Symbol Editor page, turn appropriate settings on or off, according to your preferences.

To modify the colors of screen elements and fonts used in the Block Editor window, in the Category list, select Colors or Fonts under Block/Symbol Editor. Turn appropriate settings on or off in corresponding pages.

Click OK.

You can also view larger or smaller portions of the file with the Zoom Tool, which is available by clicking the Zoom Tool button on the toolbar, and with the Zoom, Zoom In, Zoom Out, and Fit in Window commands (View menu).

To enter **input and output pins**, follow these steps:

Click the Symbol Tool button on the toolbar. The same Symbol dialog box that you used to enter the DFF, DFFE, and mult symbols appears. Note, however, that using the toolbar button opens this dialog box with the Repeat-insert mode option turned on. When Repeat-insert mode is turned on, an outline of the selected symbol remains attached to the pointer, regardless of how many times you click the mouse pointer, allowing you to place multiple copies of the symbol easily. Whenever you want to stop placing copies of a symbol, you can press Esc or choose Cancel (right button pop-up menu).

In the Symbol dialog box, in the Libraries list, click the + icon to expand the d:/quartus/libraries folder, expand the primitives folder, and then expand the pin folder.

In the pin folder, select the input (or output) primitive.

Click OK.

Click an empty space in the BDF. Symbols are automatically named as pin_name<number> in sequence. Press Esc.

Choose Save (File menu).

To **name the input and output pins**, follow these steps:

With the Selection and Smart Drawing Tool, double-click the default pin_name pin name of the first input pin symbol you entered.

You can also specify the pin name by double-clicking the pin, and then specifying the pin name in the General tab of the Pin Properties dialog box.

Repeat steps 1 and 2 to rename each of the pins

Move the INPUT and OUTPUT pin symbols so they line up with the appropriate symbols or blocks.

Choose Save (File menu).

To continue making bus **connections**, follow these steps:

Click the Orthogonal Bus Tool button on the toolbar.

Draw the bus.

Choose Save (File menu).

2b) Diseño VHDL: (vhd)

Choose New (File menu). The Device Design Files tab of the New dialog box appears automatically.

Select VHDL File.

Click OK. A new Editor window opens.

Choose Save As (File menu). The Save As dialog box appears.

Select the folder where you want to save the BDF. The Save As dialog box should automatically display the project directory name, d:\altera\qdesigns<version number>\fir_filter, as the directory for saving the file.

Make sure Add file to current project is turned on.

To save the file and add it to the project, click Save.

Write VHDL code.

3) Compilación

The Quartus II Compiler consists of a set of independent modules that check the design for errors, synthesize the logic, fit the design into an Altera device, and generate output files for simulation, timing analysis, software building, and device programming. The basic Compiler consists of the Analysis & Synthesis, Fitter, Assembler, and Timing Analyzer modules.

To **select the target device**, follow these steps

Choose Device (Assignments menu). The Device page of the Settings dialog box appears.

In the Family list, select your family. Click Yes if you are asked whether you want to allow the QuartusII software to select a device and remove any pin assignments.

Under Target device, select Specific device selected in "Available devices" list.

Under Show in "Available devices" list, select the following options:

Package list.

Pin count list.

Speed grade list.

In the Available devices list, select your device. Leave the Settings dialog box open for the next step.

The **Compilation Process Settings** page allows you to specify options that affect compilation speed, the amount of disk space used for compilation, incremental compilation, and other options.

To specify compilation process settings, follow these steps:

In the Settings dialog box, select Compilation Process Settings in the Category list. The Compilation Process Settings page appears.

To make subsequent recompilations run faster, turn on Use Smart compilation.

Make sure the Preserve fewer node names to save disk space option is turned on. Leave the Settings dialog box open for the next step.

The **Analysis & Synthesis Settings** page of the **Settings** dialog box allows you to optimize the Analysis & Synthesis processing of the design.

To specify Analysis & Synthesis settings, follow these steps:

In the Settings dialog box, select Analysis & Synthesis Settings in the Category list. The Analysis & Synthesis Settings page appears.

To direct the Compiler to maximize performance rather than device resources during Analysis & Synthesis, select Speed under Optimization Technique. Leave the Settings dialog box open for the next step.

The **Fitter Settings** page allows you to specify options that control device fitting and compilation speed. You can turn on options in this dialog box to direct the Fitter to optimize the placement of logic in order to meet your timing goals and/or options for iterative compilations.

To specify Fitter settings, follow these steps:

In the Settings dialog box, select Fitter Settings in the Category list. The Fitter Settings page appears.

Under Timing-driven compilation, make sure Optimize timing and Optimize hold timing are turned on, and make sure IO Paths and Minimum TPD Paths is selected in the list.

Under Fitter effort, select Standard Fit.

In the Settings dialog box, click OK. When you run the Compiler, these settings will control compilation processing.

Pin assigment

To generate the project database, choose Start > Start Analysis & Synthesis (Processing menu). The Compiler checks the design files for syntax and semantic errors, synthesizes the logic, and generates a project database. Click OK when Analysis & Synthesis is complete.

Choose Pins (Assignments menu). The Assignment Editor appears with the Pin assignment category selected.

In the Assignment Editor, double-click the To cell and scroll down to select any of the pin name.

In the Assignment Editor, double-click the Location cell and scroll down to select any of the dedicated clock I/O pins.

Close the Assignment Editor, saving the assignment changes.

To check the legality of the pin assignment before compilation, choose Start > Start I/O Assignment Analysis (Processing menu). When you receive a message indicating that I/O assignment analysis completed successfully, click OK to close the message box.

Compilation **((**.inc**) (**.mif**) (**.hex**) (**.qpf**) (**.qsf**))**

choose Start Compilation (Processing menu).

To view any section of the **Compilation Report**, follow these steps:

In the left pane of the Compilation Report window, click the + icon to expand any Report window folder.

In the left pane of the Report window, select the Report section you want to open. The report appears in the right pane of the window.

4) Simulación

Before running a simulation, you must specify input vectors as the stimuli for the Quartus II Simulator. The Simulator supports input vector stimuli in the form of a Vector Waveform File (**.vwf**), Vector Table Output File (**.tbl**), Power Input File (**.pwf**), or a MAX+PLUS II generated Vector File (**.vec**) or Simulator Channel File (**.scf**).

To create a VWF, follow these steps:

Choose New (File menu). The New dialog box appears.

To select VWF as the file type, click the Other Files tab and select Vector Waveform File.

Click OK. The Waveform Editor opens, displaying an empty waveform file.

To change the end time for the file, choose End Time (Edit menu).

Click OK.

To save the file as fir.vwf, choose Save As (File menu). The Save As dialog box appears.

Click Save.

To add the input and output nodes to the VWF, follow these steps:

To find the node names you want to add to the file, choose Utility Windows > Node Finder (View menu). The Node Finder appears.

In the Node Finder, select Pins: all in the Filter list.

To find the nodes you want to add to the VWF, click List.

In the Nodes Found list, select your pins and drag them into the Name column of the VWF. You can select multiple contiguous names with Shift+Click or select multiple non-contiguous names with Ctrl+Click.

Close the Node Finder.

Options

Choose Value > Arbitrary Value (right button pop-up menu). The Arbitrary Value dialog box appears.

In the Radix list, select Unsigned Decimal.

Value > Forcing Low

Value > Forcing High

To specify Simulator settings, perform the following steps:

Choose Settings (Assignments menu). The Settings dialog box appears.

In the Category list, select Simulator. The Simulator page appears.

In the Simulation mode list, make sure Timing is selected.

In the Simulation input box, type D:/altera/qdesigns<version number>/fir_filter/fir.vwf, or click Browse (...) to select the file.

Under Simulation period, make sure Run simulation until all vector stimuli are used is selected.

Make sure Automatically add pins to simulation output waveforms and Simulation coverage reporting are turned on.

Click OK. When you run the Simulator, these Simulator settings control simulation processing.

To run the simulation, follow these steps:

Choose Start Simulation (Processing menu).

To view the Simulation Waveforms section:

If necessary, in the left pane of the Simulator Report window, select Simulation Waveforms. The Simulation Waveforms section appears in the right pane of the Report window.

To see the entire waveform, choose Fit in Window (View menu).

The Waveform Editor allows you to manipulate the data in the following ways:

- You can change the radix used to display group values by selecting a group, choosing **Properties** (right button pop-up menu), and selecting a new radix in the **Radix** list.
- You can move the master time bar right and left to successive transitions by clicking the movement arrows. You can also drag the master time bar by its handle.
- You can zoom in and out with the Zoom Tool button on the toolbar, and with the **Zoom In**, **Zoom Out**, **Fit in Window**, and **Zoom** commands (View menu).
- You can create additional time bars and use them to measure distances between transitions.

5)Programación

After a successful compilation, you can download configuration data into a device through the MasterBlaster, ByteBlasterMV, ByteBlaster II, or USB-Blaster communications cables, or through the Altera Programming Unit (APU).

You can program or configure devices in Passive Serial mode, Active Serial Programming mode, JTAG mode, or In-Socket Programming mode. The following tutorial module explains how to program a single device in Passive Serial mode, as well as how to set up a multi-device JTAG chain.

To open the Programmer window, create a CDF and program the device, follow these steps:

Choose Programmer (Tools menu). A new CDF opens in the Programmer window automatically listing the filtref.sof file as the current programming file.

Choose Save As (File menu). The Save As dialog box appears.

In the Save as type list, make sure that Chain Description File is selected.

Click Save. If you are asked to replace an existing CDF, click Yes.

In the Mode list of the Programmer window, select JTAG.

Click Hardware Setup. The Hardware Setup dialog box appears.

Click Add Hardware. The Add Hardware dialog box appears.

In the Hardware type list, select ByteBlasterMV or ByteBlaster II or MasterBlaster and, if necessary, select the port and baud rate in the Port and Baud rate lists.

Click OK.

Click Close.

Configure the UP1 or UP2.

In the Programmer window, click Start. When you receive a message indicating that the configuration is complete, click OK.

Choose Save (File menu).